ABSTRACT OF THE DISCLOSURE

Various embodiments of a voltage level detector implemented as an integrated circuit whose trip point is approximately constant over variations in temperature as well as variations in transistor fabrication parameters are disclosed along with a differential amplifier whose input offset voltage is highly immune to said variations. In one embodiment, a voltage generator supplies a composite voltage to the gate of the tail current transistor of the voltage level detector or differential amplifier. The first component of the voltage is approximately equal to the threshold voltage of NMOS transistors comprised in the device over variations in operating temperature as well as variations in transistor fabrication parameters while the second component is approximately constant with respect to said variations. When applied to the gate of the tail current transistor, the first component may turn the transistor on in spite of the above-mentioned parametric variations.